Designing of the Digital Combination Lock System

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Thesis submitted in partial fulfillment of the requirements for the Degree of Bachelor of Science In Physical sciences Faculty of Applied Sciences Sabaragamuwa University of Sri Lanka Buttala. July, 2005

Declaration

The research work described in this thesis was carried out by myself at the labouratory of Faculty of Applied Sciences, under the supervision of Mr. Lasantha Aponsu (Senior lecturer, Faculty of Applied Sciences, Sabaragamuwa University of Sri Lanka).

A report on this has not been submitted to any other university for another degree.

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31/08/2005

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Affectionately Dedicated to My Family and Whoever helped me in my life

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Abstract

In present world people have seen to be prompted towards more and more sophisticated devices because of their advantageous features and simplicity. Digital combination lock is an electrically powered electronic device that can be used to provide more convenient way in a operation like opening a door instead of using a mechanical lock as used widely. In constructing such a device basic electronic components like Integrated Circuits (IC) diode, transistor, capacitors logic gates are assembled in to a single unit and to automate the unit computer programs are integrated.

Digital combination lock posses a number of advantageous features such as Remote controlling facility through network or Internet, Resetting of numbering codes, Keyless handling facility, Extended life time, Security over mechanical lock and so on.

Main objective of this project is to design a digital combination lock in order to provide more convenient way in a operation like opening a door instead of using a mechanical lock and to overcome the drawbacks of presently available locks. In addition study about the logic gates and their functioning as well as study about the practical way of implementing digital combination lock also aimed.

Basically, using CMOS ICs, Transistors, Capacitors, Resistors and PB switches interface circuit was constructed in order to transfer data from computer to the electrical equipment to be controlled through port program and usual functioning of the circuit was examined.

Since this system has wire connection it can only be used within a limited extent. If IR radiations or radio waves are used instead of wire connection it could be used even for far extent. Just as if it can improve the security further it will be enhanced the value of this system.

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CHAPTER 01

Introduction

1.1. Background

Digital circuits play a very important role in today's electronic systems. They are employed in almost every face of electronics, including communications control, instrumentation, consumer products and of course computing. This widespread usage is due mainly to the availability of inexpensive interacted circuit packages that contain powerful digital circuitry. The circuit complexity of a digital chip ranges from a small number of logic gates to a complete computer or to a quarter of a billion bits of memory.

No other area of engineering has developed faster than that of digital IT design. Over the past of years, the number of components on a digital IC chip has doubled nearly every year. (Micro electronic circuit)

In present world people have seen to be prompted towards more and more sophisticated devices because of their advantageous features and simplicity. Digitalcombination lock is an electrically powered electronic device that can be used to provide more convenient way in a operation like opening a door instead of using a mechanical lock as used widely. In constructing such a device basic electronic components like Integrated Circuits (IC) diode, transistor, capacitors logic gates are assembled in to a single unit and to automate the unit computer programs are integrated.

Digital combination lock passes a number of advantageous features.

- Remote controlling facility through network or Internet.
- Resetting of numbering codes.
- Digital combination lock is a keyless lock hence it is not needed to carry a key in hand as it is necessary in mechanical lock.
- Lift time of a mechanical lock is limited because it will be deteriorated by the time once it is used.
- Security over mechanical locks.

1.2. Objectives

- 1. To design a digital combination lock in order to provide more convenient way in a operation like opening a door instead of using a mechanical lock.
- 2. To develop a digital combination locks to overcome the drawbacks of presently available locks.
- 3. To study about the logic gates and how it functions.
- 4. To study about the practical way of implementing digital combination lock.

CHAPTER 02

Theoretical Background

2.1. What is a diode?

Diodes are among the oldest and most widely used electronic device. A diode may be defined as a near unidirectional conductor, where state of conducting is determined by the polarity of its terminal voltage diode formed by the metallurgical junction of p-type and n-type materials.

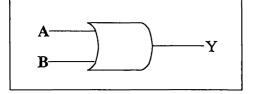
2.2. Basic digital building blocks

The digital IC building blocks to be described in this include logic gate, flip flops and latches, inverters and buffers, transceivers, multiplexes and data selectors, arithmetic circuits counters registers and memory device. A positive logic system is assumed during discussion unless mentioned otherwise in a positive logic system. More positive of the two voltage levels represents a logic "1". In a negative logic system on the other hand more positive of the two voltage levels represent logic "0". (Maini, 1996)

2.3. Logic gates

2.3.1. OR - gate

Figure 2.1 show the logic symbol and the functional table (also called the TRUTH TABLE) of a 2-input OR – gate expressed by the Boolean expression Y = A+B and read as y equal A or B. In general the output of an OR – gate is logic "0" only when all its inputs are logic "0". For all the other possible input combination the output is logic "1".

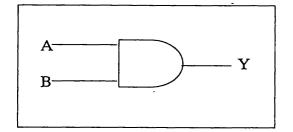


A	В	Y
0	0	0
0	1	1
1	0	1
1	1	1

Fig.2.1. Logic Symbol and Truth Table of OR - gate

2.3.2. AND - gate

Figure 2.2 shows the logic symbol and the functional table of a 2-input AND – gate expressed by y = A.B and read as y equals A and B. In general, the output of an AND – gate is logic "1" only when all its inputs are logic "1". For all other input combinations, the output is logic "0".



А	В	Y
0	0	0
0	1	0
1	0	0
1	.1	1

Fig. 2.2. Logic Symbol and Truth Table of AND – gate

2.3.3. NOT – gate

Figure 2.3 shows the logic symbol and the functional table of NOT – gate. The NOT circuit is also known as an INVERTER circuit. It complements the input that is a logic "0" at the input yields a logic "1" at the output and vice versa.

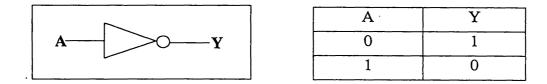


Fig. 2.3. Logic Symbol and Truth Table of NOT – gate

2.3.4. NAND – gate

Figure 2.4 shows the logic symbol and the functional table of a NAND – gate expressed by y = A.B. In general, the output of a NAND – gate is logic "0" only when all its inputs are logic "1". For all other input combinations, the output is a logic "1". Complementing the output of an AND – gate yields NAND – gate. The reverse is also true.

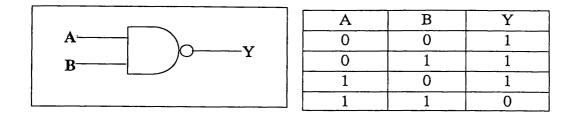
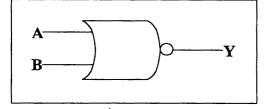


Fig. 2.4. Logic Symbol and Truth Table of NAND – gate

2.3.5. NOR - gate

Figure 2.5 shows the logic symbol and the functional table of a NOR – gate expressed by y = A+B. In general, the output of a NOR – gate is logic "1" only when all its inputs are logic "0". For all other input combinations, the output is logic "0". Complementing the output of a NOR – gate yields an OR – gate. The reverse is also true.



A	В	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 2.5. Logic Symbol and Truth Table of NOR – gate

2.4. Transistor

A junction of transistor is simply a sandwich of one type of semi-conductor material (p-type or n-type) between two layers of the other type. A block representation of a layer of n-type material between two layers of p-type is shown in figure 2.6. This is described as a pnp transistor. Figure 2.7 shows an npn transistor, consisting of a layer of p-type material between two layers of n-type. For reasons which will be understood layers, the center layer is called the base, one of the outer layer is termed as emitter and the other outer layer is referred to as the collector. The emitter, base and collector are provided with terminals, which are appropriately labeled E, B and C. Two p-n junctions exist within each transistor. Those are the collector-base junction and the emitter-base junction. (Electronic device and circuits)

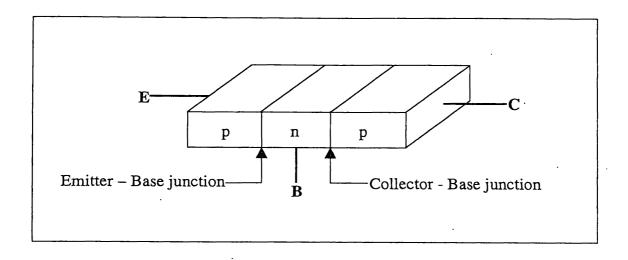


Fig. 2.6. pnp transistor

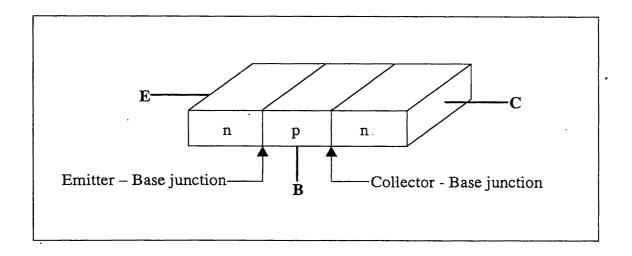


Fig. 2.7. npn transistor

Figure 2.6 is a pnp transistor, which consist of a piece of n-type material sandwiched between two pieces of p-type. In an npn transistor the center material is p-type and the two outer layers are n-type.

Circuit symbol s for pnp and npn transistor are shown in figure 2.6 and 2.7, together with the corresponding block representation. The arrowhead on each symbol always identifies the emitter terminal of the transistor. Also in each case its direction

indicates the conventional direction of current flow, for the npn transistor, the arrowhead point from the p-type base to the n-type emitter. For the pnp transistor, it points from the p-type emitter towards the n-type base. Thus, the arrowhead is always from p to n.

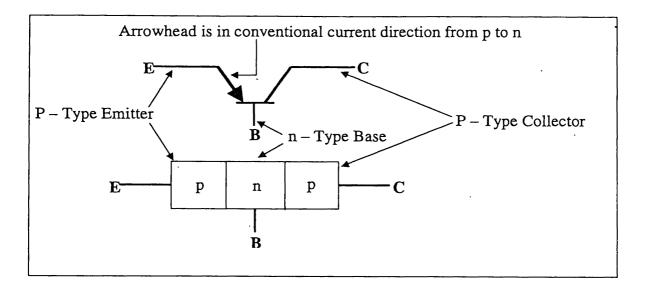


Fig. 2.8. pnp transistor for block representation and circuit symbol

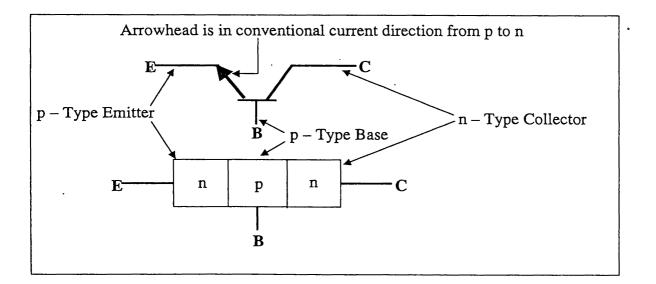


Fig. 2.9. npn transistor for block representation and circuit symbol

In the circuit symbols for pnp and npn transistor respectively the arrowhead is always at the emitter terminal and always point in the direction of conventional current flow.

2.5. CMOS Logic family

The basic difference between different CMOS logic sub families such as 400A series, 400B series, 400UB series, 74C series etc. is in the fabrication process used and not in the design of the circuit used to implement the intended logic function. Figure 2.10 to 2.11 show the circuit schematics of the basic CMOS inverter NAND – gate and NOR – gate respectively. 4000A series CMOS ICs were the first to arrive the scene from the CMOS logic family. 400A CMOS sub-family is obsolete now and has been replaced by 4000B and 4000UB sub-families. 4000B series is a high voltage version of 4000A series and also all the outputs in this series are buffered 4000UB series is also a high voltage version of 4000A series but here the outputs are not buffered.(Adel and Kenneth, 1998)

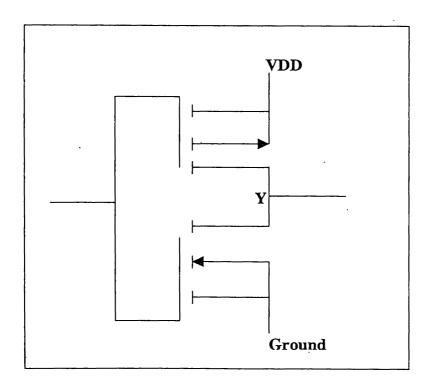


Fig. 2.10. Circuit schematics of the basic CMOS inverter NAND - gate

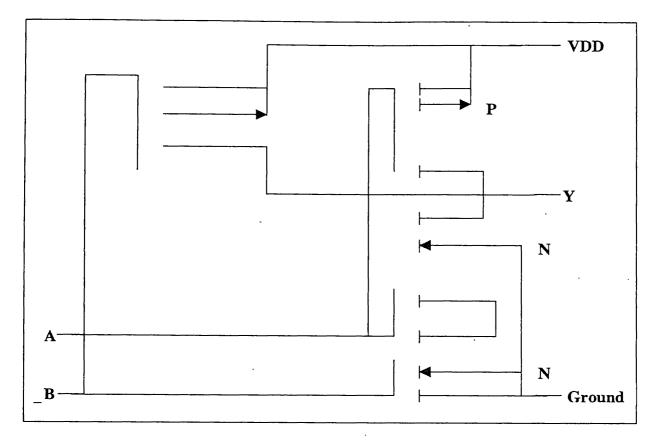
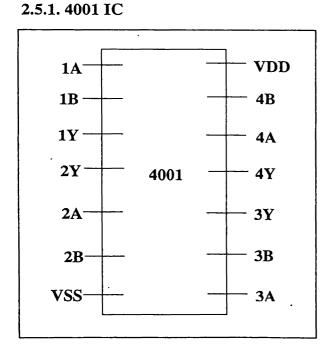


Fig. 2.11. Circuit schematics of the basic CMOS inverter NOR - gate



- **nA**, **nB** Data input
- **nY** Data output
- Y = (A+B)

A	В	Y
0	0	1
0	1	0
1	1	0
1 ·	1	0

Fig. 2.12. Schematic of the 4001 IC and truth table

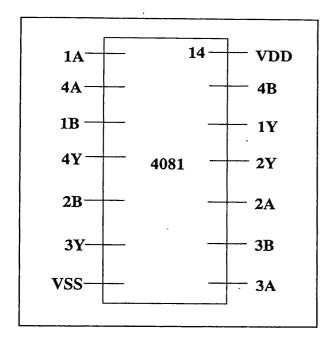


Fig.2.13. Schematic of the 4081 IC

2.5.3. 4017 IC

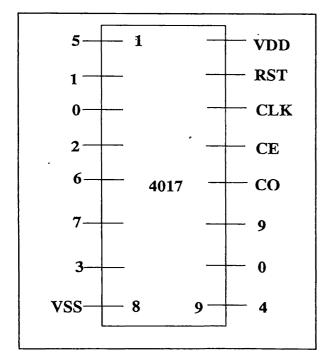


Fig. 2.14.Schematic of the 4017 IC

- **nA**, **nB** Data input
- nY Data output

• CLK – Clock

- (0-9) Decimal output
- RST Reset
- CE Clock enable
- CO Click output

Table2.1. Functional Table

RST	CE	CLK	Function
1	X	. X	Reset to "0"
0	0	1	Count
0	1	↓ ↓	Count

Table2.2. Count sequence table (Maini ,1996)

0	1	2	3	• 4	5	6	7	8	9	CO
1	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	0	0	1.
0	0	0	0	.0	1	0	0	0	0	0
0	0	0	0	0	0	1.	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	· 0	1	0	0
0	0	0	0	0	0	0	0	0	1	0

2.6. Capacitor

It is well known that different bodies hold different charge when given the same potential. This charge holding property of a body is called capacitance or capacity of the body. In order to store sufficient charge, a device called capacitor is purposely constructed. A capacitor essentially consists of two conducting surfaces (say metal plates), separated by an insulating material (e.g.: air, mica, paper, etc.). It has the property to store electrical energy in the form of electrostatic charge.

The capacitor can be connected in a circuit. so that, this stored energy can be made to flow in a desired circuit to perform a useful function. Capacitance plays an important role in D.C. as well as A.C. circuits. In many circuits (e.g.: radio and television circuits), capacitors are intentionally inserted to introduce the desired capacitance. The following points may be noted usefully.

- (1) The ability of a capacitor to store charge depends upon the area of plats, distance between plats and the nature of insulating materials. (or dielectric)
- (2) A capacitor is generally named after the dielectric used. e.g.: air capacitor, paper capacitor, mica capacitor, etc.
- (3) The capacitor may be in the form of parallel plates concentric cylinder or other arrangement. (Mehta, 1996)

2.6.1. How does a capacitor store charge?

Figure 2.15 shows how a capacitor stores charge when connected to a D.C. supply. The parallel plate capacitor having plates A and B is connected across a battery of V volts as shown in figure 2.15(a) with the switch S open as shown in figure 2.15(b), the capacitor plates are neutral that is there no charge on the plates. When the switch is closed as shown in figure 2.15(b), the electrons from plate A will be attracted by the positive terminal of the battery and these electrons start accumulating on plate B. The electrons cannot flow from plate B to as there is insulating material between the plates. Hence electrons detached from plate A start pilling up on plate B. The result is that plate A attains more and more positive charge and plate B gets more and more negative charge. This action is referred to as charging a capacitor because the capacitor plates are becoming charged. This process of electron flow or charging (that is detaching electrons from plate A and accumulating on B) continues till p.d. across capacitor plates becomes equal to battery voltage V. when the capacitor is charged to battery voltage V the current flow causes as shown in figure 2.15(c). If now the switch is opened as shown in figure 2.15(d) the capacitor plates will retain the charges. Thus the capacitor plates, which were neutral to start with how, have charges on them. This shown that a capacitor stores charges. (Metha, 1996).

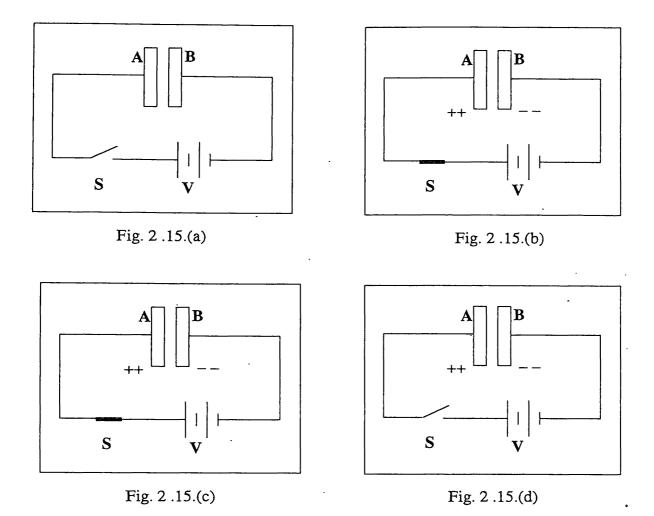


Fig 2.15. How a capacitor stores charge when connected to a D.C. supply.

2.7. Resistance

The opposition offered by a substance to the flow of electric current is called resistance.

Since current is the flow of free electrons, resistance is the opposition offered by the substance to the flow of free electrons. This opposition occurs because atoms and molecules of the substance obstruct the flow of these electrons. Certain substances (eg: metals such as silver, copper, aluminum, etc.) offer very little opposition to the flow of electric current and are called conductors. On the other hand, those substance which of high opposition to the flow of electric current (i.e. flow of free electrons), are called insulators eg: glass, rubber, mica, dry wood, etc.(Theodore and Bogart, 1995).

2.7.1. Factors upon which resistance depends

The resistance R of a conductor

- (1) is directly proportional to it's length
- (2) is inversely proportional to it's area of cross section
- (3) depends upon the nature of material
- (4) changes with temperature

From the first three points (leaving temperature for the time being), we have

$$\frac{R \alpha 1/a}{R = \rho 1/a}$$

Where ρ is a constant and is known as resistance of the material. It's value depends upon the nature of material (David, 1999).

2.8. The switches

The switching of an active device is a non-linear operation that places the device in one of two basic states for controlled period of time.

(01) An "on" state corresponding to a condition of heavy condition.

(02) An "off" state corresponding to condition of light condition.

In practical electronic switches in the on state consists of a range of output voltage $0 < V_0 < V_L$ (called low logic). The off state consists of the range $V_L < V_H < V_0$. Power supply voltage (called high logic) V_L is called to the low logic limit and V_H the high logic threshold. Subsequent circuitry must be capable of discriminating effectively between V_L and V_H .

CHAPTER 03

Materials and Methodology

3.1. Materials

- Breadboard and breadboard sockets
- Four 4017 CMOS IC
- Eight 4001 CMOS IC
- Four 4081 CMOS IC
- Four 22n Capacitors
- Three 100n Capacitors
- Four 220n Capacitors
- Four P.B. Switches
- 9 volt heavy- duty battery
- Two 2.2 KΩ resistors
- Five 10 KΩ resistors
- Four 100 KΩ resistors
- Four $1M\Omega$ resistors
- BC182B Transistor
- LED

3.2. Methodology

- Foremost Breadboard was taken which is 8" in length and 4" in width, and divided in to four equal size parts. Those were nominated as A, B, C and D respectively. (Figure 3.1)
- Each part comprises;
 - 1. P.B switch
 - 2. 22n capacitor
 - 3. 220n capacitor
 - 4. Two 10 KΩ resistors
 - 5. 100 KΩ resistor
 - 6. $1M\Omega$ resistor
 - 7. 4017 IC
 - 8. 4001 IC

- To construct part A Press Button Switch A (P.B.S), 4001 two COMS ICS, 4017 CMOS IC and Other parts listed above which are the components have to be assembled to part A were fixed on the bread board as shown in (Figure 3.2) below.
- Likewise same sets of components were fixed for another three parts (B, C, D) also.
- There after four each part was connected through 4081 ICs. (Figure 3.3)
- 10KΩ resistor was fixed serially to the RESET button.
- When part D was connected to the external circuits, 2.2 KΩ Resistor was linked to base of the BC182B transistor, while connector linked to out put and emitter was earthed.
- LED and 2.2 KΩ Resistor, that are in serial format were connected externally to the part D, as it is parallel. (Figure 3.4)
- Connected the ground (0V) and pin number 7 of every IC s to the middle bus of the breadboard.

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Fig 3.1. View of Breadboard

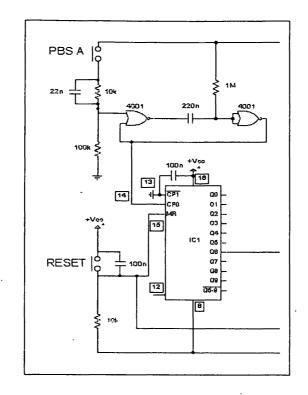


Fig 3.2. Assembling of Circuit components of part A

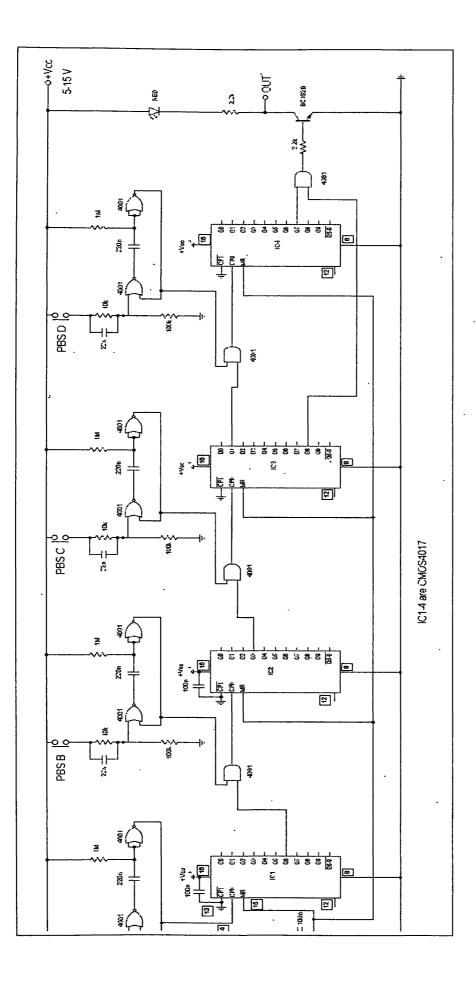


Fig 3.3. Overall Circuit

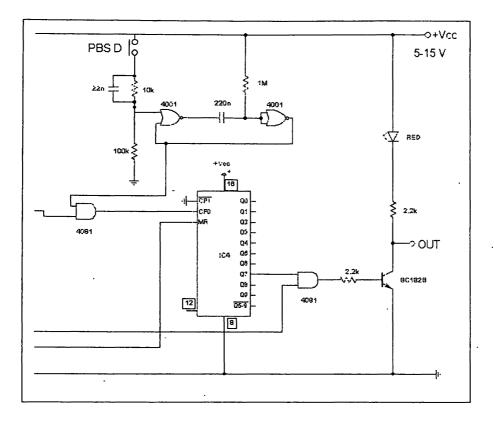


Fig 3.4. Connection between part D and External Circuit

CHAPTER 04

Discussion and Conclusion

People in this era always go for whatever easy for them to do. So, people tend to find ways to control devices remotely. The main objectives of developing a Digital Combination Lock is to control devices remotely without controlling them manually and improve the convenience in controlling.

There are several advantages of this system. If we use traditional method of opening a door, we always have to take the key of the door wherever we go and also the key might be weared along with time. Also each person who wishes to enter the room has to have a common key separately. The most interesting part of this system is that, any door or window can be opened using a few digital numbers, without using any key. Also this enables access to the specified room by people who knows the exact code number and no common key is further needed. This also gives a protection from robberies because spare keys won't function in opening the door.

IC was connected to the computer with the use of printer port. This printer port enables the instruction flow from computer to the IC. The instruction mentioned above related to a collection of data, which was written in C or Pascal programming language. This data helps to implement a task such as opening a door or window in another location, or switching a television or a radio only by giving instructions manually to the computer. But to carry out this task, printer port connection between computer and IC is a prerequisite. Also there should a connection to the internet or any information flow regarding the task to the computer using Pascal or java, or C language.

But one of a disadvantage that occur when implementing this system is that, if the data or command were given to the given to the computer through Internet, we cannot assure about the security of the system. Since anyone who have a knowledge in Pascal or C can access to the Internet readily and implement the operation. In this system the 104n capacitors were used instead of 22n capacitors. The reason for this was the tolerance to the temperature by 22n capacitor was lower than the 104n capacitor.

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CHAPTER 05 Recommendations

Since, this system has wire connections, there are some limitations. This system can only be built within a limited extension. If this system developed to operate using IR radiations or radio waves, the limited extent could be expanded.

Also if the security system could be enhanced or improved, the significance of this system will be higher.

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References

Adel, S.S. and Kenneth, C.S. (1998) Microelectronic Circuits, Oxford University Press, 4th Ed, 1237p.

David, A.B. (1999) Electronic devices and circuits, Prentice-Hall, 3rd Ed.756p.

Maini, A.K., (1996), Handbook of electronics, Khanna publishers, 2nd Ed, 951p.

Mehta, V.K., (1996) Principles of Electrical Engineering And Electronics, S.Chand and Company Limited , 1st Ed, 721p.

Theodore, F. and Bogart, J., (1995) Electronic Devices and Circuits, University of Southern Mississippi. 847p.

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